Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of making a multiple gate electrode on a semiconductor device, comprising the steps of:

coating a layer of gate electrode material over top and past the opposed sides of a semiconductor device that has been previously coated with a thin film of gate dielectric on the top and the opposed sides of the semiconductor device; and

planarizing the layer of gate electrode material to produce a substantially planar surface formed only of the gate electrode material disposed atop the semiconductor device and extending distally past each of the opposed sides, prior to patterning the gate electrode material to form a discrete multiple gate electrode on the semiconductor device, the substantially planar surface having the same height at locations superjacent the semiconductor device and at locations distal the semiconductor device.

2. (Currently Amended) The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness and a planar top surface on the planar top surface of the planarized gate electrode material including directly over the semiconductor device;

patterning the photoresist mask to cover a corresponding pattern of the discrete multiple gate electrode; and

etching the gate electrode material that is uncovered by the photoresist mask to form the discrete multiple gate electrode.

3. (Original) The method of Claim 1, further comprising the step of:

conforming the layer of gate electrode material with a step height increase corresponding to an increased step height of the semiconductor device.

4. (Original) The method of claim 1, wherein the semiconductor device comprises a silicon fin

5. (Original) The method of claim 1 wherein, the semiconductor device comprises a fin of silicon and germanium.

6. (Currently Amended) The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness and a planar top surface on the planar top surface of the planarized gate electrode material including directly over the semiconductor device, the mask comprising photoresist and a mask material selected from the group comprising, silicon nitride, silicon oxynitride, silicon oxide and photo resist, or combinations thereof;

patterning the photoresist mask to cover a corresponding pattern of the multiple gate electrode; and

etching the gate electrode material that is uncovered by the photoresist mask to form the discrete multiple gate electrode.

7. (Currently Amended) The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness and a planar top surface on the planar top surface of the planarized gate electrode material including directly over the semiconductor device;

patterning the photoresist mask to cover a corresponding pattern of the multiple gate electrode; and

plasma etching the gate electrode material that is uncovered by the photoresist mask to form the patterned multiple gate electrode.

8. (Original) The method as recited in claim 1, further comprising the step of: applying a mask over the planarized surface, wherein the mask is of substantially uniform thickness for accurate patterning thereof.

9. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon oxide.

10. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon oxynitride.

11. (Original) The method of claim 1 wherein, the gate dielectric comprises a high permittivity material.

12. (Original) The method of claim 1 wherein, the gate dielectric comprises a material having a permittivity greater than 5.

13. (Original) The method of claim 1 wherein, the gate dielectric comprises a thickness in the range of 3 and 100 Angstroms.

14. (Original) The method of claim 1 wherein, the multiple gate electrode comprises polycrystalline silicon.

15. (Original) The method of claim 1 wherein, the multiple gate electrode comprises a conductive material.

16. (Original) The method of claim 1 wherein, the multiple gate electrode comprises a metal material.

17. (Currently Amended) A semiconductor device having a multiple gate electrode, comprising:

the semiconductor device having a projecting fin coated with a gate dielectric film over top and opposed sides of the fin;

a multiple gate electrode on each of the opposed sides of the fin, the multiple gate electrode formed of a layer of gate electrode material and having a substantially planar surface disposed atop the gate dielectric film formed over the top of the fin and extending distally past each of the opposed sides of the fin; and

a patterned mask on the planar surface of the multiple gate electrode, the patterned mask having a substantially uniform thickness and a substantially planar surface including over the fin.

18. (Previously Presented) The semiconductor device of claim 17 wherein, the multiple gate electrode is a portion of the layer of gate electrode material which has a planarized surface that includes the planar surface of the multiple gate electrode.

19. (Cancelled)